J. Electr. Electron. Mater.
Vol. 38, No. 5, pp. 513-520 September 2025
doi: https://doi.org/10.4313/JEEM.2025.38.5.6
ISSN 1226-7945(Print), 2288-3258(Online)

Regular Paper

Electrical Properties Based on the Number of Stacked Layers for the Optimal Design of BaTiO-Based MLCCs for MIL-PRF-32535 Compliance

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(Received February 11, 2025; Revised February 26, 2025; Accepted February 27, 2025)

Abstract: Multilayer ceramic capacitors (MLCCs) are essential for high-capacitance, miniaturized, and reliable electronic applications. This study examines the impact of layer stacking on the dielectric and electrical properties of MLCCs using a $BaTiO_3$-based dielectric with MgO, Mn_3O_4, Yb_2O_3, V_2O_5, and $(BaCa)SiO_3$ glass additives. MLCCs with 10 um-thick dielectric layers and varying Ni electrode layers (10, 30, 50, and 100 layers) were fabricated. The dielectric constant increases significantly up to 30 layers due to compressive stress and sintering densification but it becomes linear beyond 30 layers. Dissipation factor and ESR decrease with higher stacking due to improved sinterability, while breakdown voltage declines exponentially from defect accumulation and thermal stress. Insulation resistance decreases but stabilizes relative to capacitance. C-V results show stress-induced polarization suppression, which reduces the dielectric constant under high voltage. Optimized stacking and sintering conditions are crucial for MIL-PRF-32535 compliant MLCC designs.

Keywords: $BaTiO_3$, MLCC (multilayer ceramic capacitor), Compressive stress, MIL-PRF-32535 compliant

1. INTRODUCTION

Multilayer ceramic capacitors (MLCCs) are essential components in modern electronic devices, serving functions such as power supply stabilization, signal filtering, and energy storage. As industries such as artificial intelligence (AI), electric vehicles (xEVs), and next-generation communication technologies (6G) continue to advance, the demand for miniaturized, high-efficiency components with stable electrical properties under high-temperature and high-voltage conditions has grown significantly. Consequently, there has been a surge in demand for high-capacity MLCCs that meet stringent reliability standards [1,2]. High-capacitance MLCCs primarily utilize $BaTiO_3$-based dielectrics, classified as Class II materials due to their high dielectric constant. However, $BaTiO_3$, a ferroelectric material, exhibits nonlinear dielectric properties and flexoelectric effects that vary with voltage and temperature. When integrated into MLCCs, its dielectric properties can be altered due to interactions with internal electrodes during fabrication. To achieve high capacitance, MLCCs require an increased number of thinner dielectric and electrode layers, with Ni or Cu commonly used as internal electrode materials. The sintering process for these materials requires a reducing atmosphere to prevent oxidation, and additives such as Mn_3O_4, MgO, rare-earth oxides (e.g., Yb_2O_3, Dy_2O_3, Y_2O_3), V_2O_5, and SiO_2 are employed to mitigate oxygen vacancy formation in the dielectric. A key challenge in MLCC design and manufacturing is managing residual stress, which arises due to differences in thermal expansion coefficients and shrinkage rates between dielectric and

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electrode layers during the sintering process. Residual stresses, including compressive and tensile stress, significantly impact MLCC reliability by influencing the electric field distribution, defect formation, insulation resistance, breakdown voltage, and temperature coefficient of capacitance (TCC). Mechanical defects such as cracks and delamination, induced by residual stress, can degrade the long-term reliability of MLCCs, which is particularly critical for aerospace and military applications requiring compliance with the MIL-PRF-32535A standard [3,4]. Despite ongoing research on MLCC performance optimization, there remains a gap in understanding the correlation between practical manufacturing processes and key electrical properties, such as dielectric constant, capacitance-voltage (C-V) characteristics, insulation resistance, and TCC. Previous studies have indicated that increasing the number of stacked layers induces compressive planar residual stresses or non-planar tensile stresses, which can influence dielectric properties. However, a comprehensive analysis linking structural parameters with electrical performance is still lacking [5-9]. In this study, the objective is to design and manufacture MLCCs that comply with the MIL-PRF-32535A standard, focusing on the relationship between structural parameters and electrical performance. MLCCs with a dielectric composition exhibiting X8R characteristics (EIA-198 standard, operating temperature range: -55°C to +150°C, and capacitance variation within ±15% over this range) were designed and fabricated. The effects of the stacking layer count on dielectric and electrical properties were systematically investigated to optimize MLCC performance while ensuring compliance with the MIL-PRF-32535A standard. By analyzing the relationship between structural stress distribution and electrical characteristics, this study aims to contribute to the development of high-capacity, high-reliability MLCCs for advanced electronic applications.

2. EXPERIMENTAL

In this study, a dielectric material capable of sintering in a reducing atmosphere was employed to achieve X8R characteristics. The dielectric composition used $BaTiO_3$ (KCM, Japan) as the main component, with MgO, Mn_3O_4, Yb_2O_3, V_2O_5, and $(BaCa)SiO_3$ glass powder as additives. The dielectric raw materials were mixed and dispersed using a Nano-Set Mill along with PVB binder, ethanol/toluene, dispersant, and plasticizer to produce a slurry. The slurry was then used with a coater to fabricate 10 μm-thick green sheets on a release PET film. Ni internal electrodes were printed onto the green sheets, which were subsequently stacked, laminated, and sintered in a reducing atmosphere at 1,260°C for 2 hours. Post-sintering, the chips were heat-treated at 1,000°C for 1 hour, and Cu external electrodes were applied and heat-treated at 800°C to complete the MLCCs. The fabricated MLCCs had a 2012 form factor (2.0 mm length, 1.2 mm width) with stacking layers of 10, 30, 50, and 100. For comparison, K-square samples with zero stacking layers (no internal electrodes) were also prepared to examine the dielectric properties. The crystal phases of the samples were analyzed using X-ray diffraction (XRD, BRUKER AXS D4 ENDEAVOR), and the internal microstructures were observed using field-emission scanning electron microscopy (FE-SEM, JSM-9701, JEOL, Japan). These analyses allowed for the evaluation of post-sintering dielectric layer thicknesses and microstructures. The dielectric properties were measured using an LCR meter (HP 4284A) at 1.0 kHz and 1.0 Vrms to determine the dielectric constant, dissipation factor, and equivalent series resistance (ESR). Insulation resistance was measured using a high resistance meter (HP 4339B) after applying a voltage of 4 V/μm for 60 seconds. The breakdown voltage per unit thickness was evaluated using a dielectric withstand tester (HIOKI 3174). In this test, the temperature chamber was used to apply a DC voltage at a rate of 0.5 V/sec until the leakage current reached 1μA, which was defined as the breakdown criterion. The temperature coefficient of capacitance (TCC) was measured across a temperature range of -25°C to 150°C at a measurement frequency of 1 kHz using an LCR meter (HP 4284A) in a temperature-controlled chamber.

3. RESULTS AND DISCUSSION

Figure 1 shows the X-ray profiles of the number of layers at the center of MLCCs with varying dielectric layers. The X-ray profiles for the (200) reflections in $BaTiO_3$ were compared among MLCCs with different dielectric layer counts. A shift of the (200) peak toward lower angles is observed as the number of dielectric layers increases. This shift suggests an

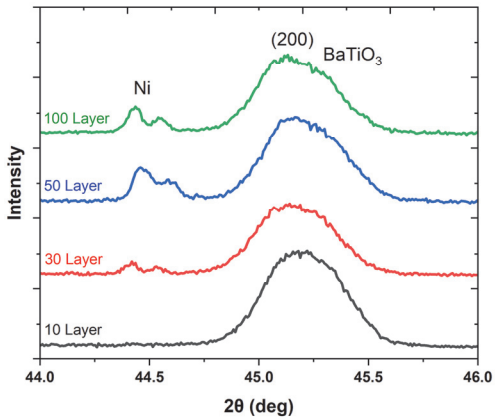

Fig. 1. X-ray diffraction profiles of MLCCs with different number of dielectric layer.

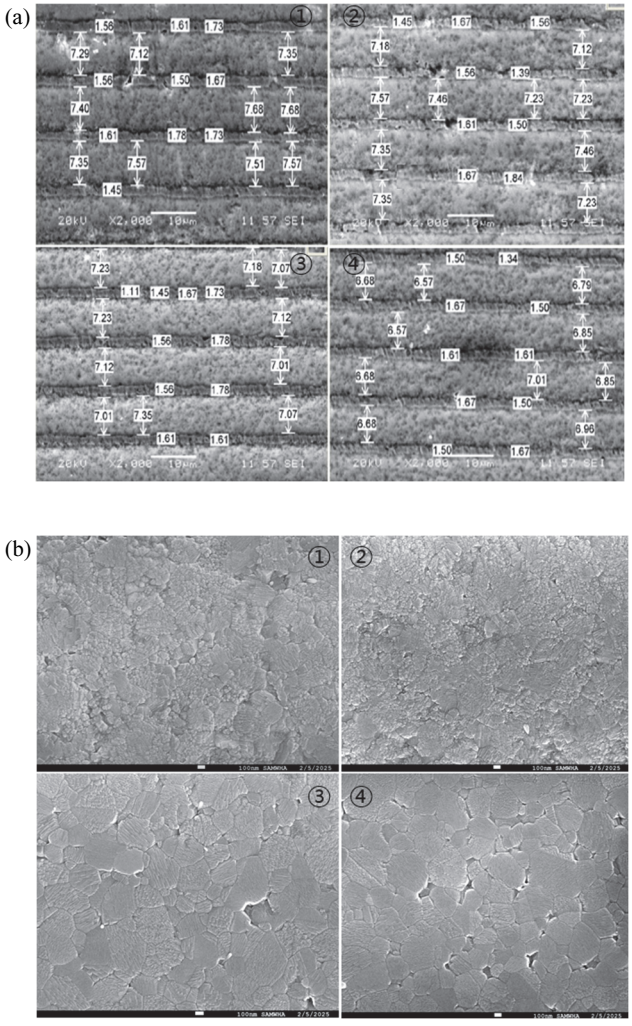

Fig. 2. SEM of MLCCs with different number of dielectric layer sintered in a reducing atmosphere at 1,260°C for 2 hours. SEM image of the internal electrode and dielectric and (b) SEM image of the dielectric.

expansion of the lattice parameter, which is directly influenced by internal stresses within the MLCC structure. The c-axis orientation is expected to result from tensile stress in the thickness direction. These results are likely due to stress caused by the difference in thermal expansion coefficients between the ceramic material BaTiO and the Ni metal electrodes, which exhibit different shrinkage rates during the sintering and cooling processes. In general, Ni electrodes shrink more than $BaTiO_3$, inducing compressive stress within the $BaTiO_3$ structure. This stress is likely responsible for the observed changes in lattice spacing. Considering the sintering characteristics, it is also inferred that grain size has a combined effect on these results.

Figure 2 shows the SEM images of MLCCs with different numbers of dielectric layers. Figure 2(a) presents the cross-sectional images of the dielectric and internal electrodes, illustrating the variation in electrode thickness with increasing layer numbers. The average thickness of the internal Ni electrode exhibits a slight change from 1.6 μm to 1.58 μm as the number of layers increases. In contrast, the average dielectric thickness decreases from 7.4 μm to 6.6 μm, indicating a reduction trend as the layer count increases. Figure 2(b) displays the microstructure of the dielectric layer, where an increase in the number of layers leads to grain growth in the $BaTiO_3$ dielectric. Notably, for MLCCs with more than 50 layers, uniform grain growth is observed. This phenomenon is attributed to the increase in the Ni/$BaTiO_3$ interface with increasing layer numbers. During the sintering process, the Ni interface acts as a diffusion path, and due to the high diffusion coefficient of Ni, it enhances the mobility of atoms and vacancies within $BaTiO_3$. This facilitates sintering, resulting in an increased shrinkage rate. Furthermore, in MLCCs with more than 50 layers, uniform grain growth occurs because rapid mass transport at the Ni interface equalizes the driving force for grain growth within the $BaTiO_3$ dielectric during sintering. This leads to the promotion of normal grain growth (NGG) rather than abnormal grain growth (AGG), ensuring a homogeneous microstructure [10].

Figure 3 illustrates the change in dielectric constant with the number of layers in MLCCs. The dielectric constant was

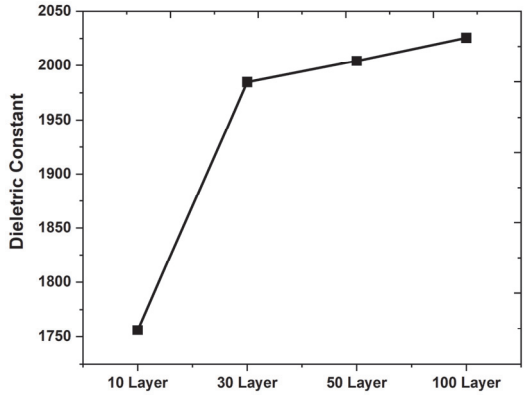

Fig. 3. The dielectric constant of MLCCs with different number of dielectric layer sintered in a reducing atmosphere at 1,260°C for 2 hours.

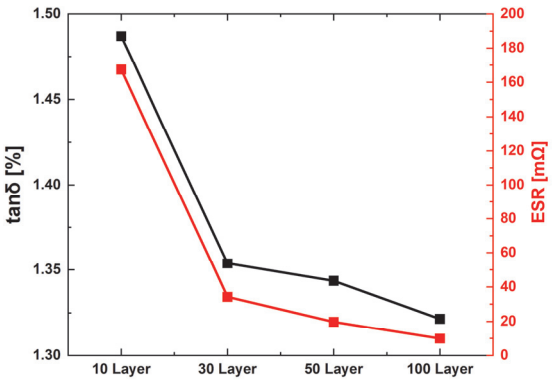

Fig. 4. The dissipation factor and ESR characteristics of MLCCs with different number of dielectric layer sintered in a reducing atmosphere at 1,260°C for 2 hours.

calculated after measuring the capacitance of the MLCCs, taking into account the dielectric thickness and the effective area, including the coverage of internal electrodes. For a 10-layer structure, the dielectric constant is approximately 1,750, which closely matches the value of 1,725 observed for the dielectric fabricated without internal electrodes. However, for the 30 layer structure, the dielectric constant sharply increases to 1,980. As the number of layers increases to 50 and 100, the dielectric constant continues to rise, albeit at a more gradual rate. It is generally known that the dielectric constant of high-permittivity materials is influenced by the microstructure and density of the sintered body. Based on the results shown in Fig. 1, the shrinkage rate, which is closely related to sintering density, tends to increase with the number of layers. This suggests that the presence of Ni internal electrode layers impacts the sintering process and contributes to the increase in the dielectric constant. The sharp rise in the dielectric constant observed when transitioning from 10 to 30 layers can be attributed to domain effects induced by internal stress. Specifically, the residual stress in $BaTiO_3$ alters its crystal structure, elongating the c-axis while contracting the a-axis, thereby increasing the c/a ratio. This trend is corroborated by XRD analysis results [6,7]. The increase in the dielectric constant with additional layers is believed to be due to compressive stress enhancing domain reorientation, promoting the transformation of 90° domains, and increasing their mobility [11,12]. From a microstructural perspective, the grain size and stress distribution also influence domain wall mobility, leading to an increase in the dielectric constant. These findings align with previous studies suggesting that the mobility of domain walls is a critical factor in enhancing the dielectric properties.

Figure 4 presents the dissipation factor and ESR characteristics as a function of the number of layers in an MLCC. These properties are critical indicators of the electrical performance of the dielectric, representing energy loss during polarization processes within the dielectric. The dissipation factor, primarily caused by energy losses during the polarization process, is closely related to capacitance, frequency, and impedance of the dielectric, as described by Eq. (1).

$$\tan\delta = \frac{R_S}{\omega C} \quad (1)$$

Where, tanδ: Dissipation factor (dielectric loss), Rs: Equivalent series resistance (ESR), ω=2πf, Angular frequency, C: Capacitance.

As the number of layers increases, the dissipation factor is observed to rise. This trend is similar to the sharp increase in dielectric constant shown in Fig. 3, where the dissipation factor exhibits a significant change from 10 layers to 30 layers. However, beyond 30 layers, up to 100 layers, there is no notable variation. The influence of polarization loss mechanisms, such as electronic polarization, ionic polarization, orientational polarization, and space charge polarization, is expected to be minimal as the number of layers increases. The reduction in dissipation factor observed with increasing layers in MLCCs is primarily attributed to

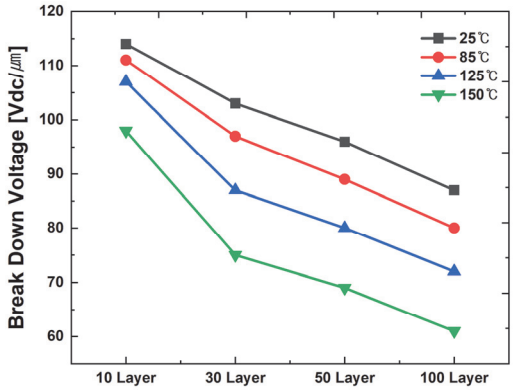

Fig. 5. The dielectric breakdown voltage per unit thickness of MLCCs with different number of dielectric layer sintered in a reducing atmosphere at 1,260°C for 2 hours.

improved sinterability as the number of layers grows. Structurally, as the number of electrode layers increases, the contact area between electrodes and the dielectric expands, leading to reduced contact resistance. Furthermore, the increased parallel stacking of internal electrodes results in a reduction of the overall equivalent resistance [13,14]. These structural improvements collectively contribute to the observed reduction in dissipation factor.

Figure 5 shows a graph of the dielectric breakdown voltage per unit thickness as a function of dielectric layer count and temperature. Regardless of the number of layers, it is observed that the dielectric breakdown voltage per unit thickness decreases as temperature increases. For layer counts of 10 and 100, the decrease in dielectric breakdown voltage per unit thickness between 25°C and 150°C is dramatically reduced from 97% to 56%. The increase in dielectric breakdown voltage per unit thickness with rising temperature is expected to be due to the increased mobility of ions at higher temperatures, which makes conduction current more likely to flow. Additionally, it is also due to the reduction in dielectric constant of $BaTiO_3$-based dielectrics with voltage, resulting in an increase in the relative electric field strength within the dielectric. The dielectric breakdown strength per unit thickness of ceramic dielectrics is fundamentally governed by the interaction between material defects—such as impurities, voids, cracks, and non-uniformities in dielectric thickness and the electric field, mechanical, and thermal stresses applied to the material. Defects in the ceramic structure serve as stress concentrators, locally amplifying the electric field intensity, which in turn reduces the dielectric strength. This localized field enhancement, combined with mechanical and thermal stresses generated during the manufacturing process, can lead to the initiation of electrical breakdown at lower voltage levels. Impurities and voids act as charge traps, while cracks can propagate under stress, contributing to dielectric failure through both electrical, thermal, and mechanical mechanisms. Consequently, these defects influence the overall breakdown strength by creating regions of weakness where the applied stress exceeds the material's intrinsic breakdown capacity [14-17]. The decrease in dielectric breakdown voltage per unit thickness with increasing layer count is exponentially increased due to the rise in defect density and internal stresses between the internal electrodes and the dielectric, as well as differences in the thermal expansion coefficients. These effects lead to a side effect (area effect), where the breakdown probability follows a Weibull distribution and decreases exponentially, as seen in Eq. (2) [18]. However, for more than 30 layers, the breakdown voltage per unit thickness decreases linearly. This behavior is similar to the change in dielectric constant with dielectric thickness shown in Fig. 3, where the effect of the increasing number of layers becomes linear after 30 layers.

$$P_{Total} = 1 - e^{-A\cdot\left(\frac{x}{\lambda}\right)^n} \quad (2)$$

P_{Total}: Total failure probability for a dielectric and inner el ectrode with area

A: Dielectric and inner electrode area

x: Scale parameter

λ: Observed variable (temperature, voltage)

m: Shape parameter

The larger decrease in dielectric breakdown voltage at higher temperatures in high-layer-count capacitors is likely due to the increased defect density and the impact of thermal stress at elevated temperatures.

Figure 6(a) presents the results of insulation resistance per unit thickness as a function of the number of layers and temperature. It is evident that as both the number of layers and the measurement temperature increase, the insulation resistance per unit thickness decreases. Conversely, Fig. 6(b) illustrates the effect of increasing the number of layers on the product of insulation resistance (IR) and capacitance (C),

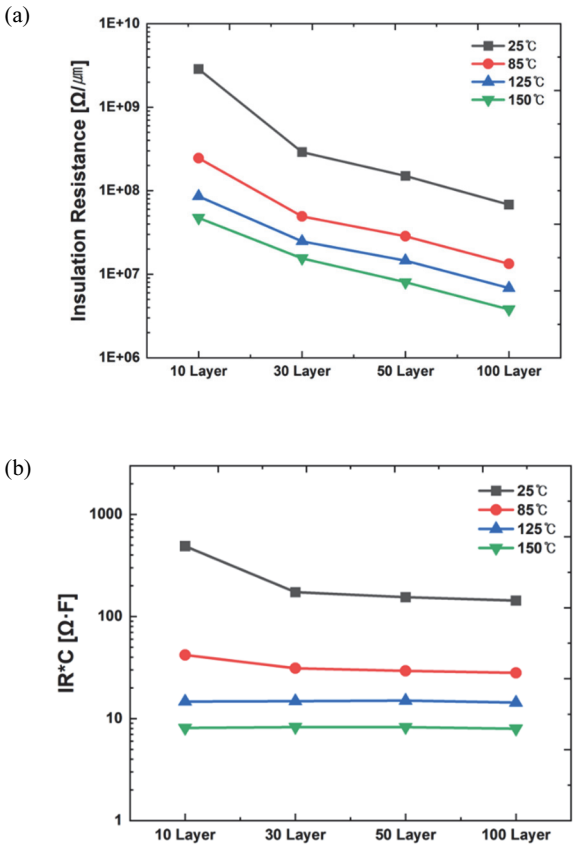

Fig. 6. The Insulation resistance and IR*C value of MLCCs with different number of dielectric layer sintered in a reducing atmosphere at 1,260°C for 2 hours. (a) Insulation resistance and (b) IR*C value.

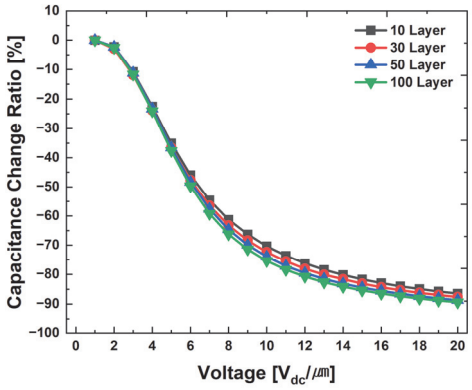

Fig. 7. C-V characteristics of MLCCs with different number of dielectric layer sintered in a reducing atmosphere at 1,260°C for 2 hours.

where the increase in the number of layers does not significantly affect the insulation resistance, despite the increase in capacitance. According to the relationship IR·C = ρ·ε (where ρ denotes resistivity and ε denotes permittivity), the change in capacitance resulting from an increase in the number of layers influences the permittivity, yet exerts minimal impact on the reduction of insulation resistance. In general, the decrease in insulation resistance in MLCCs with high permittivity is attributed to defects and polarization effects induced by ion mobility, whereas in MLCCs sintered in a reducing atmosphere, oxygen vacancies within the dielectric material enhance conductivity [19-22]. From the results in Fig. 6(b), the absence of significant differences in IR·C values, despite the increase in capacitance with the number of layers, suggests that the reduction in insulation resistance due to the stacking of layers is less impactful than the influence of resistivity ρ and capacitance C. Furthermore, while insulation resistance per unit thickness must be considered in the design of MLCCs with an increasing number of layers, the increase in capacitance resulting from the increase in permittivity indicates that for designs involving more than 30 layers, both the insulation resistance per unit thickness and the IR·C values must be incorporated into the MLCC design.

Figure 7 illustrates the C (capacitance)-V (voltage) characteristics as a function of the number of layers. As the number of layers increases, the changes in the C-V characteristics become more significant with higher applied voltage per unit thickness. This phenomenon can be attributed to the alignment of the ferroelectric spontaneous polarization in the direction of the applied electric field as the voltage per unit thickness increases, leading to a decrease in the dielectric constant and, consequently, a reduction in the capacitance. These characteristics are strongly influenced by the thickness and composition of the dielectric material. The greater change in capacitance with applied voltage as the number of layers increases is attributed to the suppression of polarization response caused by the alignment of BaTiO crystal structure along the c-axis under stress, as seen in Fig. 3, which illustrates the increase in dielectric constant due to stress. In general, for Class II MLCCs, the movement of $BaTiO_3$ domain walls under DC voltage results in a decrease in the dielectric constant. To mitigate this effect, improvements are achieved by incorporating rare-earth elements or Mn into nano-powder $BaTiO_3$, which minimizes defects within the dielectric [23].

Figure 8 shows the TCC (temperature coefficient of capacitance) characteristic curves as a function of the number

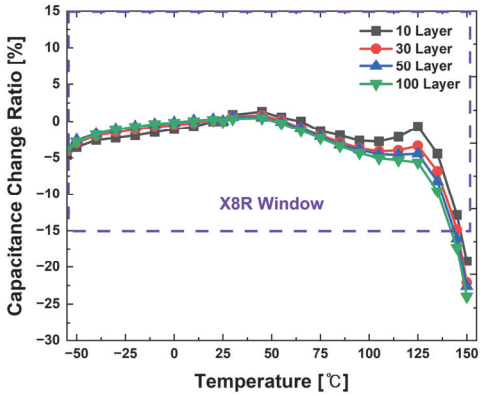

Fig. 8. TCC characteristics of MLCCs with different number of dielectric layer sintered in a reducing atmosphere at 1,260°C for 2 hours.

of layers, exhibiting a TCC characteristic within ±15% over the temperature range of -55°C to 150°C. The composition used in this experiment is based on the $BaTiO_3$-MgO-Mn_3O-Yb_2O_3-V_2O_5-(BaCa)SiO_3 system, with a dielectric thickness of 10 μm after sintering, which achieves X8R characteristics. However, as shown in Fig. 2, when the dielectric thickness is reduced to 6~7 μm after sintering, X8R characteristics are not observed. As the number of layers increases, a phase transition near the Curie temperature of $BaTiO_3$ (approximately 125°C) begins, resulting in a decrease in spontaneous polarization. In Fig. 3, similar to the dielectric constant characteristics, the TCC shows a significant change at 30 layers compared to 10 layers, while beyond 30 layers, it exhibits a similar trend. This behavior is presumed to be caused by the increased temperature sensitivity of the crystal structure due to residual stress.

4. CONCLUSIONS

This study examined the effects of layer stacking on the dielectric and electrical properties of MLCCs with a $BaTiO_3$ based dielectric composition, optimized for X8R characteristics. The results show that increasing the number of stacked layers significantly influences key properties. The dielectric constant increases notably up to 30 layers due to compressive stress enhancing domain wall mobility and sintering densification but becomes linear beyond this point. The dissipation factor and ESR decrease with higher layer counts due to improved contact resistance and structural uniformity. However, breakdown voltage per unit thickness decreases exponentially with increasing layers, driven by defect accumulation, thermal stress, and localized electric field enhancement. Insulation resistance decreases with more layers but stabilizes relative to capacitance (IR•C), highlighting its minimal impact on overall performance. The C-V characteristics reveal stress-induced suppression of polarization, leading to a reduction in dielectric constant under higher applied voltage. TCC analysis confirms X8R performance for 10 μm-thick dielectrics but shows limitations when the thickness decreases further. These findings emphasize the critical role of residual stress and defect control in optimizing MLCC designs, ensuring compliance with MIL-PRF-32535A standards for high-temperature and high-reliability applications.

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ACKNOWLEDGEMENT

This work was supported by the Technology Innovation Program (RS-2024-00430833, Development of MLCC commercialization technology for automotive electronics an alternative to rare earth for high reliability response) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea).

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