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Multilayer Ceramic Capacitors for AI Servers and Data Centers: Challenges, Reliability Issues, and Future Technology Directions

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Abstract:. The rapid proliferation of artificial intelligence (AI) servers and high-performance computing systems has significantly elevated the technical and reliability requirements for multilayer ceramic capacitors (MLCCs). In such systems, MLCCs are critical passive components that must deliver high capacitance, fast transient response, and robust insulation performance under high temperature, voltage, and current density. This review examines the material, structural, and process innovations that underpin MLCC performance in AI applications. Key topics include the development of ultrathin dielectric layers (<0.5 μm), rare-earth doped $BaTiO_3$-based dielectrics with enhanced DC bias stability, and core–shell microstructures designed for temperature and field resilience. The paper also explores insulation degradation mechanisms—such as vacancy-driven conduction and demixing—and advanced reliability assessment methodologies, including HALT, TSDC, and the tipping point framework. Comparisons with automotive-grade MLCCs highlight the unique requirements of AI systems, such as ultra-miniaturization, high volumetric efficiency, and ppm-level field failure rates. Finally, the review discusses emerging trends in MLCC technology, including particle engineering, interface stabilization, and advanced lamination techniques, and provides insight into the future direction of capacitor development tailored to AI data center environments.

Keywords: Multilayer ceramic capacitors, AI servers, $BaTiO_3$, Core–shell dielectric, DC bias stability, Insulation resistance, Reliability testing

1. INTRODUCTION

The rapid advancement of artificial intelligence (AI) has led to an unprecedented surge in computing demands required for large-scale data processing, high-speed inference, and the operation of generative models. To meet these demands, high-performance parallel processors—such as GPUs (graphics processing units), NPUs (neural processing units), and ASICs (application-specific integrated circuits)—have become the core computing resources in modern data centers and AI servers. However, as state-of-the-art AI accelerators consume hundreds to thousands of watts (W) per module, a fundamental redesign of power system architectures and component selection is essential [1-3]. Figure 1 shows the NVIDIA GH200 Grace Hopper Superchip, a representative heterogeneous computing platform that integrates an Arm-based Grace CPU and an H100 GPU based on the Hopper architecture into a single module. This superchip is widely used not only in high-performance computing (HPC) applications—such as high-precision simulations, computational fluid dynamics, and quantum chemistry calculations—but also in large-scale computing workloads across data

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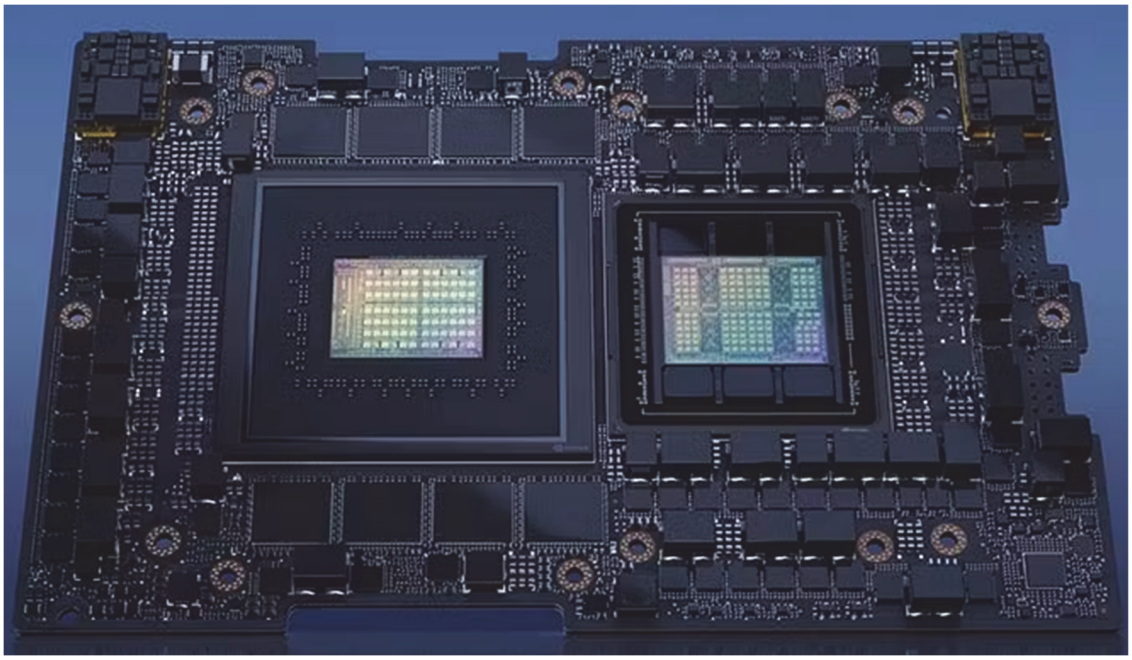

Fig. 1. NVIDIA GH200 Grace Hopper Superchip.

centers and supercomputing environments, including data-parallel processing, AI model inference, and big data analytics.

Figure 2 illustrates a power supply unit (PSU) board employing a hybrid-switched capacitor converter (DR-HSC) topology, specifically designed for data center applications [4]. This example showcases an evaluation board implementing a 48 V-to-12 V converter based on a zero-voltage switching (ZVS) switched capacitor (ZSC) architecture. In AI systems, PSUs are increasingly required to deliver output power exceeding 3–4 kW. These high-power supplies incorporate multiple power conversion stages that must provide fast transient current response within microseconds. Under such high-speed switching and high-power operation, maintaining system stability and minimizing voltage ripple become critical design challenges [5-7]. MLCCs, as essential passive components, play a crucial role in securing power integrity. They fulfill multiple functions simultaneously, including power rail noise suppression, peak current buffering, high-frequency filtering, and voltage smoothing. The key performance requirements for MLCCs in these PSU applications are summarized in Table 1. Accordingly, MLCCs have a direct influence on both the reliability and energy efficiency of AI computing systems.

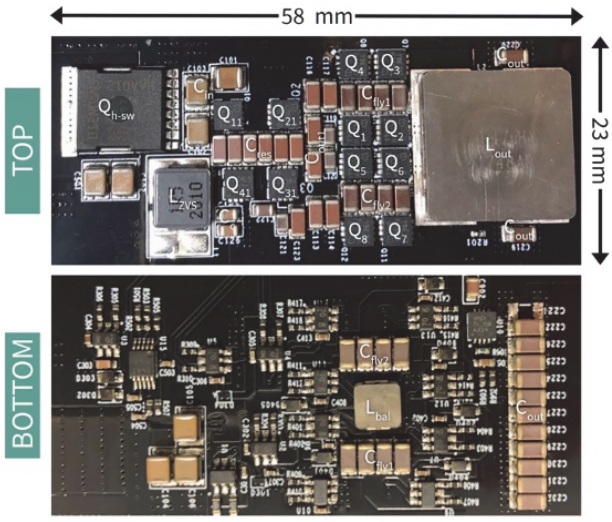

Fig. 2. An evaluation board for a 48 V-to-12 V hybrid-switched capacitor converter (DR-HSC) designed for high-power data center applications.

Compared to MLCCs used in consumer electronics or industrial equipment, MLCCs for AI applications must achieve extreme miniaturization, high capacitance, and elevated reliability within stringent space and thermal constraints. For example, a single GPU-based AI board may incorporate more than 10,000 MLCCs, each required to

Table 1. Functional roles of MLCCs and corresponding technical requirements in PSU applications.

Function	Required MLCC characteristics	Technical description
High-frequency filtering	High capacitance, low ESR/ESL	Suppresses MHz-range switching noise; SRF (self-resonant frequency) must lie in high-frequency band.
Voltage smoothing	High voltage rating, wide thermal stability	Bulk MLCCs needed to suppress output voltage ripple in 48 V-to-1 V conversion; X7S/X7R class recommended.
Peak current compensation	High pulse current (di/dt durability)	Must supply transient current within microseconds under dynamic load; large-size MLCCs used in parallel.
Noise suppression	Low dissipation factor, low loss, high reliability	Meets EMI/EMC requirements; requires high Q-factor and stable dielectric materials.
Thermal stability	Class I or thermally stabilized Class II dielectric	Maintains performance under PSU heat and temperature fluctuation

support rapid charge-discharge cycles and maintain thermal stability in a limited mounting area. Depending on their application, MLCCs in AI systems can be classified into two main categories. The first type includes high-voltage MLCCs used in PSU circuits such as LLC resonant and snubber circuits. These capacitors must maintain excellent insulation and stable temperature characteristics (e.g., X7S, C0G) at rated voltages ranging from several hundred to several thousand volts. The second type comprises high-capacitance MLCCs operating at 4 V or higher, typically mounted near the power pins of processors such as GPUs, CPUs, or TPUs, and often rated at 47 μF or more in ultra-compact form factors. The explosive growth of the AI server and GPU board markets is driving a significant surge in demand for MLCCs. Unlike those used in consumer or industrial electronics, MLCCs integrated into AI systems must simultaneously meet stringent requirements for miniaturization, high capacitance, and high reliability under severe spatial and thermal constraints. In practice, a single GPU-based AI board can incorporate over 10,000 MLCCs, highlighting the enormous demand. Each component must deliver rapid charge/discharge performance and thermal stability within a limited mounting area. MLCCs are placed in close proximity to the processor power pins to respond to rapid load transients during AI operations, compensating for instantaneous peak currents and stabilizing voltage levels. These capacitors are mounted near high-performance processors such as GPUs, CPUs, and TPUs, and are required to operate at low rated voltages exceeding 4 V, while achieving high capacitance values of 47 μF or more in ultra-compact form factors [8-10]. MLCCs are passive components used in electronic circuits to perform functions such as charge storage, DC blocking, filtering, coupling, frequency discrimination, and circuit tuning. Their performance characteristics are determined by parameters such as capacitance, rated voltage, temperature characteristics (TCC), and physical size. Among these, temperature characteristics are particularly important and are classified according to industry-standard codes defined by the Electronic Industries Alliance (EIA), which specify the allowable temperature range and capacitance variation. For example, Class I dielectrics (e.g., C0G) feature very low temperature coefficients of capacitance (TCC $\leq \pm 30$ ppm/°C) over a temperature range of -55°C to +125°C, providing excellent thermal and electrical stability. In contrast, Class II dielectrics (e.g., X7R, X8R, X9R) offer higher capacitance values but with broader TCC tolerances. C0G MLCCs are especially valued in applications requiring high thermal stability and precise capacitance control under varying temperatures. For example, X7R MLCCs maintain a capacitance variation within ±15% from -55°C to +125°C, X8R extends the upper temperature limit to 150°C, and X9R is capable of operating in extreme environments up to 200°C. In these high-temperature applications, the dielectric material must exhibit temperature-independent relative permittivity to ensure stable capacitance over the entire operating range [11-13]. To meet these performance requirements, advanced material and process innovations are essential throughout the entire MLCC manufacturing workflow—ranging from dielectric formulation and internal electrodes to green sheet casting and sintering. $BaTiO_3$ remains the dominant dielectric material;

however, as dielectric layers are reduced below 1 μm in thickness, maintaining high permittivity while controlling grain size becomes increasingly challenging. Generally, smaller BT grain sizes enhance capacitance stability under DC bias but may suppress ferroelectric domain formation, thereby reducing permittivity. Hence, the use of core shell microstructures with grain sizes in the 100~200 nm range is preferred, as this configuration contributes to both enhanced permittivity and improved temperature stability. $BaTiO_3$ remains the principal dielectric material for MLCCs used in AI systems. However, as the dielectric layer thickness is reduced below 0.8 μm, it becomes increasingly difficult to maintain high permittivity while precisely controlling grain size. In general, reducing the particle or grain size of $BaTiO_3$ enhances capacitance stability under DC bias but tends to suppress ferroelectric domain formation, resulting in a decrease in dielectric constant. To address this trade-off, efforts are underway to optimize additive systems and sintering conditions in order to achieve uniform core–shell microstructures with grain sizes in the range of 100~200 nm, enabling a balanced improvement in both permittivity and temperature coefficient of capacitance [14-17]. To form the shell layer in core–shell structures, dopants such as rare-earth elements (Dy, Y, Ho) and multivalent cations (Mg, Mn) are commonly employed. These dopants substitute into the A or B sites of the $BaTiO_3$ lattice, mitigating oxygen vacancy formation, enhancing electrochemical stability, suppressing dielectric loss, and inhibiting abnormal grain growth. In particular, co-doping with Dy and Ho promotes relaxor behavior in the shell region, attenuating the dielectric peak near the Curie temperature and facilitating compliance with specifications like X7R or X7S. When base metal electrodes (e.g., Ni, Cu) are used, sintering must occur in a reducing atmosphere, which inherently promotes oxygen vacancies that can degrade insulation resistance and reduce device lifetime. Accordingly, compositions that regulate both the concentration and mobility of oxygen vacancies (e.g., MgO, MnO_2, V_2O_5 additives) are of high research interest. To ensure the insulation resistance, lifetime characteristics, and temperature coefficient of capacitance stability in BME (base metal electrode) MLCCs, precise control over both dielectric composition and sintering processes is essential. While sintering in a reducing atmosphere is necessary to prevent oxidation of base metal electrodes such as Ni or Cu, it also induces the formation of oxygen vacancies within the $BaTiO_3$ dielectric. These oxygen vacancies act as n-type carriers, increasing electronic conductivity, degrading insulation resistance, and ultimately reducing the device's operational lifetime. To mitigate this degradation, a reoxidation process performed in a mildly oxidizing atmosphere after sintering is often employed. This step helps replenish oxygen vacancies and restore high insulation resistance. Rare-earth oxides such as Dy_2O_3, Ho_2O_3, and Y_2O_3 are particularly effective in suppressing oxygen vacancy formation and trapping free electrons, thereby maintaining a high-resistance state within the ceramic. These rare-earth dopants can substitute into either the A-site (Ba) or B-site (Ti) of the $BaTiO_3$ perovskite lattice, simultaneously improving dielectric properties, insulation durability, and long-term reliability. Co-doping with Dy and Ho promotes relaxor behavior in the shell region of the dielectric microstructure, which mitigates the temperature dependence of permittivity and helps achieve compliance with TCC specifications such as X7R or X7S. Additionally, multivalent metal oxide additives such as MgO, MnO_2, and V_2O_5 help regulate the concentration and mobility of oxygen vacancies, enhancing electrochemical stability. These dopants also suppress abnormal grain growth, contributing to refined microstructural control. Their incorporation reduces dielectric loss and plays a critical role in improving the lifespan and overall reliability of MLCCs [18-21]. Therefore, current research efforts in high-reliability BME MLCCs are focused on compositional engineering using rare-earth and multivalent dopants, optimization of reducing and reoxidation conditions, and precise control of oxygen vacancy behavior. From a process standpoint, the manufacturing of AI-targeted MLCCs also demands significant sophistication. The dielectric layer thickness has now been reduced to 300–600 nm, and the number of stacked layers has increased to several hundred. As a result, factors such as slurry dispersion stability, green sheet coating uniformity, sintering shrinkage control, dielectric-electrode interface adhesion, and post-sintering oxidation control are critical to ensuring desired electrical properties. In high-temperature, high-electric-field AI server environments, key reliability metrics include dielectric stability under DC bias, suppression of leakage current, maintenance of insulation resistance, breakdown voltage, and long-term durability verified via HALT (highly accelerated life testing). Although AI and automotive MLCCs share certain reliability

expectations, they diverge significantly in their core technical requirements. Automotive MLCCs are designed to endure extreme environments, including temperatures from -55°C to 150°C, as well as mechanical stress from vibration, flexure, and electrostatic discharge, with long-term reliability over thousands of hours. In contrast, MLCCs for AI servers prioritize ultra-miniaturization and high capacitance density, capable of responding instantaneously to frequent current peaks from GPUs. Thus, while mechanical and thermal durability are critical in automotive applications, fast charge-discharge responsiveness and field stability are central to MLCCs in AI systems. In MLCCs for AI data centers, the dielectric layer thickness has been drastically reduced to the range of 0.3~0.7 μm, resulting in extremely high electric field strengths. This degree of miniaturization introduces unique insulation resistance degradation mechanisms not typically observed in conventional MLCCs, thereby necessitating more sophisticated process control and advanced materials engineering to ensure long-term reliability. Furthermore, the increase in the number of stacked layers and the operation under high-temperature and high electric field conditions have intensified the need for precise control over several critical processes. These include slurry dispersion stability, uniformity in green sheet coating, sintering shrinkage management, improved adhesion at the dielectric electrode interface, and prevention of postsintering oxidation. Under such conditions, key reliability metrics include dielectric stability under DC bias, suppression of leakage current, maintenance of insulation resistance, securing breakdown voltage, and verification of long-term durability through Highly Accelerated Life Testing [22-26]. Although MLCCs for AI and automotive applications share certain baseline reliability requirements, their technical specifications differ significantly based on the end-use environment. Automotive MLCCs are designed to endure extreme temperature conditions ranging from -55°C to 150°C, as well as mechanical stresses such as vibration, flexure, and electrostatic discharge (ESD), with long-term reliability over several thousand hours. In contrast, AI server MLCCs prioritize ultra-miniaturization and high capacitance density, with an emphasis on rapid charge-discharge responsiveness to frequent and abrupt current surges generated by GPUs, along with excellent electric field stability. As a result, while mechanical and thermal robustness is essential for automotive MLCCs, electrical responsiveness and long-term insulation reliability are more critical for MLCCs used in AI systems. In summary, MLCCs for high-performance AI servers and data centers are evolving from traditional passive components into key enablers of rapid power response and system-level stability. This review focuses on the C–V characteristics of ultra-thin dielectric layers in AI data center environments and the degradation mechanisms associated with ensuring long-term reliability under high electric field conditions. To address these challenges, the review explores innovations in materials and processing technologies, including the structural and dielectric properties of $BaTiO_3$, rare-earth doping strategies, internal electrode design, and key advancements in manufacturing processes such as slurry dispersion control, green sheet formation, and sintering. Finally, by comparing MLCCs used in AI systems with those used in automotive applications, this work highlights the critical technical differentiators and proposes future directions for MLCC development tailored to next-generation AI infrastructure.

2. MLCC MANUFACTURING PROCESS

In advanced MLCC fabrication, slurry formulation requires nanoparticle dispersion stability to prevent agglomeration during tape casting. Uniform green sheet thickness (<1 μm) ensures consistent electric field distribution, while electrode printing must maintain precise layer alignment within 100 nm to avoid internal cracks or delamination. During sintering in reducing atmospheres, careful thermal profiling minimizes interfacial reactions between Ni electrodes and $BaTiO_3$ grains. Post-sintering reoxidation replenishes oxygen vacancies, restoring insulation resistance. Advanced lamination systems employ automated roll pressing with micro-step accuracy, critical for stacking hundreds of ultra-thin dielectric layers. Integration of simulation-based sintering shrinkage compensation further enhances structural uniformity and minimizes reliability risks. Figure 3 illustrates the manufacturing process of MLCCs (multilayer ceramic capacitors), which is based on the precise control of ultrathin dielectric and inner electrode formation, nanoparticle technologies, advanced lamination techniques, and high-temperature sintering processes. To achieve high-capacitance and high-reliability MLCCs, optimization of each

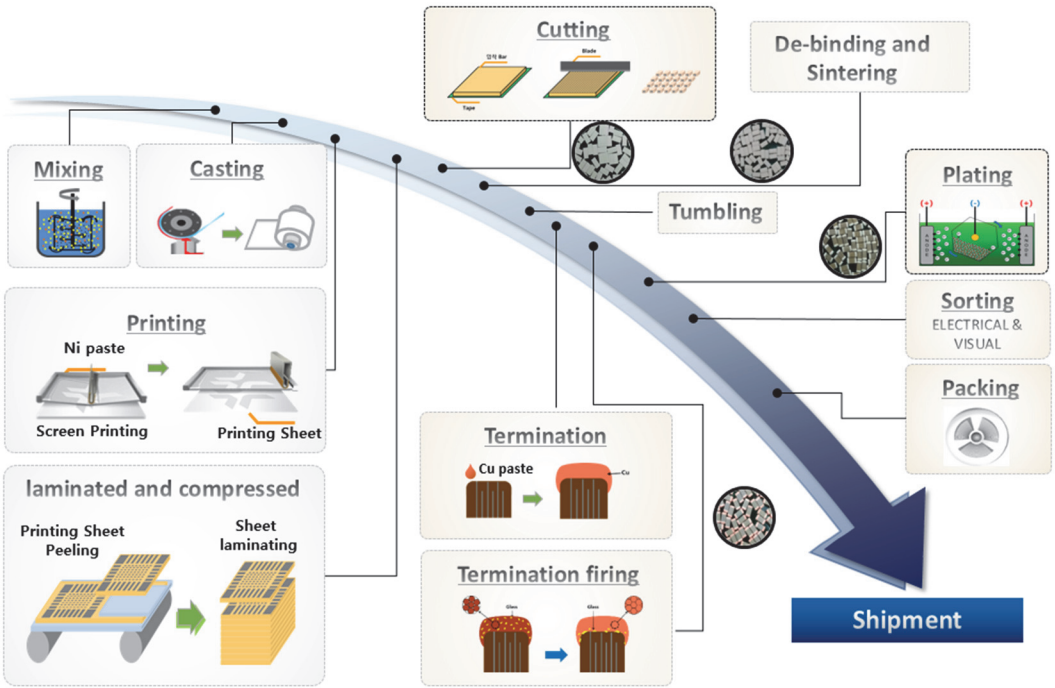

Fig. 3. A comprehensive schematic of the MLCC manufacturing process.

manufacturing step is essential. MLCCs are formed by alternately stacking dozens to hundreds of dielectric layers and inner electrode layers, and are fabricated to be compatible with surface mount technology (SMT) by connecting to external terminals. The core process begins with the preparation of the dielectric slurry, in which ceramic raw materials are finely ground and uniformly dispersed. This involves mixing $BaTiO_3$ with additives such as MgO, Mn_3O_4, Y_2O_3, Dy_2O_3, V_2O_5, and SiO_2, as well as binders, dispersants, plasticizers, and solvents using high-shear dispersion and mixing equipment. The result is a viscous slurry with sufficient flowability for tape casting in subsequent steps. The dielectric powders used are nanoscale, typically with particle sizes ranging from 50 to 300 nm, and maintaining compositional stability and dispersion homogeneity is critical to high-performance MLCC fabrication. In the tape casting and inner electrode printing step, the slurry is cast into continuous thin ceramic sheets (green sheets) with a thickness of 0.5 to 20 μm using die coater or slot-die casting methods. On these green sheets, metal pastes for the inner electrodes are printed using screen printing or gravure printing techniques. At this stage, uniformity of the printed layer thickness, rheological properties of the metal paste, mesh size of the screen, and the thickness of the emulsion layer are key factors influencing performance. The laminated and compressed forming process involves precisely aligning and stacking the required number of printed green sheets, followed by the lamination process, where heat and pressure are applied to consolidate them into a single laminated bar. Mechanical precision and alignment accuracy of the lamination equipment are crucial for forming stable multilayer stacks that can reach several hundred layers. The de-binding and sintering process begins by cutting the laminated bars into chip-sized pieces, followed by thermal treatment to remove organic binders in the de-binding step. If de-binding is not performed properly, defects such as voids, cracks, or deformation may occur, degrading product reliability. In the subsequent firing process, the dielectric and electrode layers are co-sintered in a reducing atmosphere using either batch type or continuous RHK-type furnaces at 1,000 to 1,300°C, typically through a rapid two-step sintering profile. Precise temperature and atmosphere control during sintering is required to prevent shrinkage deformation, interfacial reactions, and metal oxidation. A re-oxidation process is performed after sintering to minimize the degradation of insulation resistance. In the external terminal formation and electrical testing phase, the sintered chips undergo edge

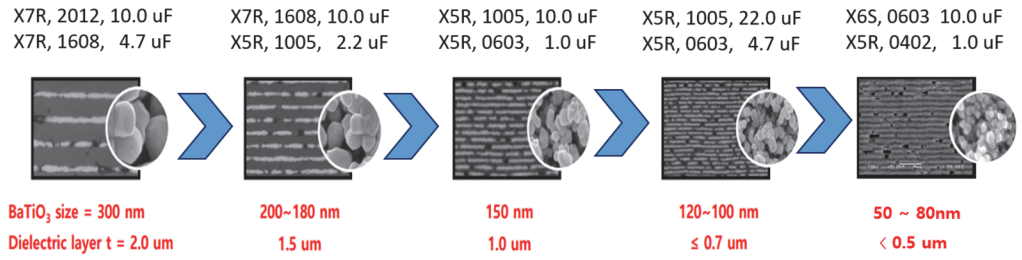

Fig. 4. The technological roadmap illustrating the evolution of MLCC volumetric capacitance density.

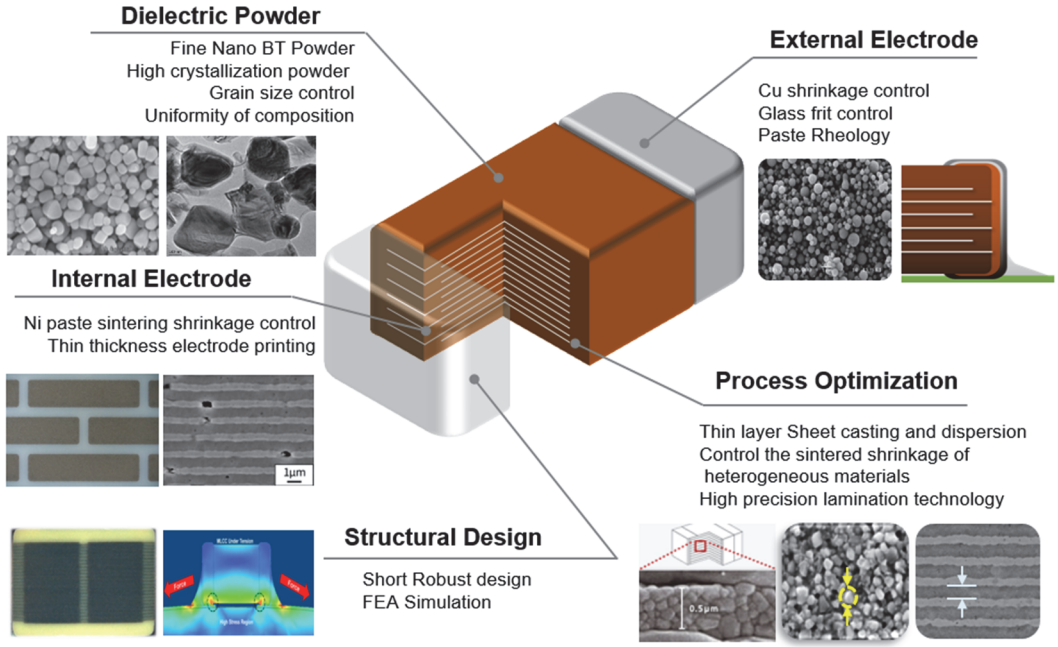

Fig. 5. An illustration of the four core synergistic technologies required for manufacturing high-density, high-reliability MLCCs.

rounding through, followed by the formation of external terminals via dipping in copper paste and subsequent firing. To ensure SMT compatibility and solderability, Ni and Sn layers are applied by barrel-type chemical or electroplating processes. Finally, the chips are subjected to full electrical inspection—testing parameters such as capacitance, insulation resistance, and breakdown voltage—to verify quality before packaging and shipment.

3. CAPACITANCE TRENDS AND CORE TECHNOLOGIES OF MLCCs

MLCCs now feature dielectric layers scaled down to several hundred nanometers and stacked in hundreds to thousands of layers, ushering in an era where even atomic-scale defects must be meticulously controlled. Figure 4 illustrates the roadmap of volumetric capacitance density as a function of dielectric particle size and layer thickness, highlighting the exponential growth trend in MLCC capacitance density over recent decades. The capacitance (C) of an MLCC is determined by the equation:

$$C = \frac{\varepsilon_r A}{d} N$$

where ε_r is the relative permittivity, A is the overlapping electrode area, N is the overlapping electrode number and d is the dielectric layer thickness. While reducing d increases

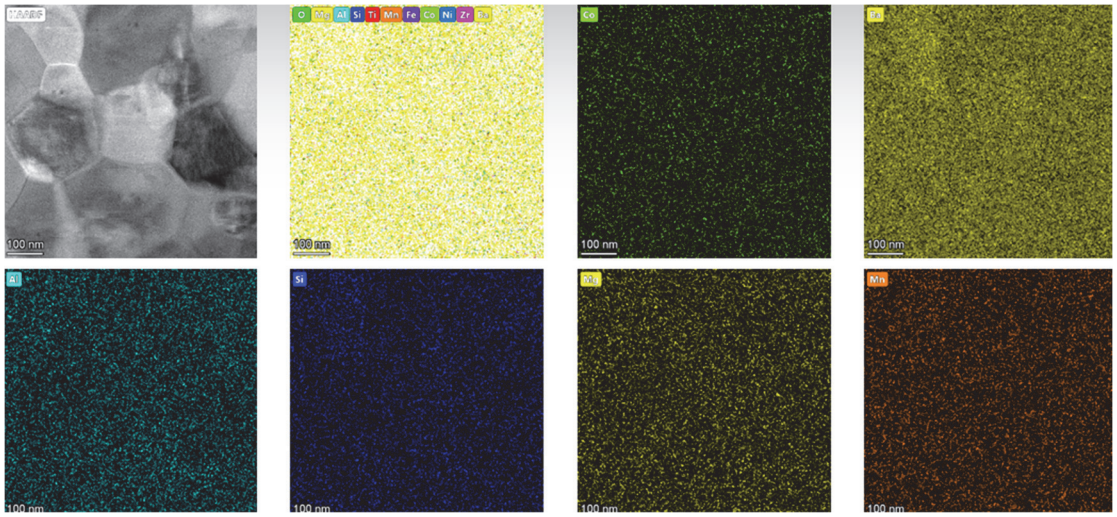

Fig. 6. High-resolution Transmission Electron Microscopy (TEM) image and corresponding Energy Dispersive X-ray Spectroscopy (EDS) elemental maps of a high-density MLCC designed for AI applications.

capacitance (C), it simultaneously raises critical reliability concerns such as dielectric breakdown, short circuits, and interfacial defects. Therefore, the realization of next-generation high-performance MLCCs requires not only nanoscale dielectric layers, but also simultaneous advancements in particle engineering, interface stabilization, and high-precision lamination technologies. These high-density integration requirements have been addressed through the synergistic development of four core technologies, summarized in Fig. 5. First, fine particle technology stems from the fact that the electrical properties of the $BaTiO_3$ based dielectric layers used in MLCCs are highly dependent on grain size and uniformity. While early MLCCs utilized $BaTiO_3$ particles with average sizes of approximately 300 nm, state-of-the-art devices now employ nanoparticles smaller than 40 nm. However, simple particle size reduction is not sufficient. During sintering, fine particles are susceptible to agglomeration and abnormal grain growth, which can cause localized electric field intensification and increase the risk of dielectric breakdown. As such, precise control over particle morphology, size distribution, and post-sintering microstructural homogeneity is essential. Second, thin-layer technology involves dispersing uniform nanoparticles into a slurry and forming them into thin green sheets, which serve as the dielectric layers. As the dielectric thickness decreases, the number of grains per layer drops from several dozen to just a few, making the device increasingly vulnerable to a single defect. Moreover, the influence of the electrode–dielectric interface becomes more pronounced, necessitating stringent control of interfacial defects. To address these issues, techniques such as core shell grain architectures, grain boundary engineering, and interface charge management have been widely adopted. Third, high-precision lamination technology is critical for stacking hundreds to thousands of ultra-thin dielectric layers alternated with Ni electrodes, all with nanometer-level accuracy. For instance, stacking 1,000 layers each 0.5 μm thick results in a component only 0.5 mm tall, requiring lamination precision better than 100 nm. This level of accuracy is achieved using advanced automation systems including micro-stepping control, precision roll pressing, and automated alignment equipment. Any accumulated misalignment during lamination can lead to serious defects such as delamination, internal cracking, or warpage during pressing and sintering, potentially resulting in catastrophic failure. Fourth, advanced materials and process technology plays a pivotal role in mitigating reliability issues associated with ultra-thin dielectric layers. Doping $BaTiO_3$ with trace amounts of rare-earth elements such as Dy, Y, and Ho suppresses grain growth and stabilizes the perovskite crystal structure, thereby improving insulation resistance and dielectric stability. This enables stable operation under high-temperature and high-electric-field conditions. Furthermore, co-firing ceramics (dielectrics) with metals (electrodes), which inherently exhibit mismatched thermal expansion

coefficients and sintering behaviors, introduces major integration challenges. To overcome this, techniques such as the application of glaze layers for shrinkage compensation, the development of low-temperature sinterable dielectrics, and simulation-based thermal profiling for process optimization have been employed. These approaches contribute to defect-free integration and enhanced reliability of MLCCs [27-30]. Figure 6 presents the microstructure of an MLCC manufactured for AI applications, analyzed using Transmission Electron Microscopy (TEM) and Energy Dispersive X-ray Spectroscopy (EDS). The high-resolution TEM image shows well-defined grain boundaries with grain sizes maintained in the range of 50 to 200 nm, indicating a tightly controlled sintering process. Elemental mapping via EDS confirms the uniform distribution of key dopants such as Mg, Mn, Si, and rare-earth elements throughout the dielectric matrix. This homogeneous dispersion is critical for achieving the desired electrical performance and long-term reliability in high-density MLCCs.

4. FUNDAMENTAL PROPERTIES OF $BaTiO_3$ For AI DATA CENTER MLCCs

Recent studies on $BaTiO_3$-based dielectrics emphasize the importance of precise particle size control (50–150 nm) to stabilize tetragonal distortion and maintain spontaneous polarization. Rare-earth dopants such as Dy, Y, and Ho substitute into A- or B-sites, reducing oxygen vacancy formation and suppressing abnormal grain growth. These mechanisms improve DC bias stability by restricting domain wall motion while simultaneously enhancing insulation resistance. Core–shell structures, where high-permittivity ferroelectric cores are surrounded by relaxor-type shells, distribute electric field stress and improve capacitance retention. Detailed in-situ TEM and spectroscopy analyses confirm that defect-dopant interactions are central to long-term stability in ultra-thin dielectric layers (<0.5 μm). Figure 7 illustrates the temperature-dependent phase transitions and dielectric constant of $BaTiO_3$. At elevated temperatures, $BaTiO_3$ undergoes a phase transition to a paraelectric state with an isotropic cubic perovskite structure, where the lattice parameters are equal (a = b = c). In this ideal centrosymmetric structure, Ba^{2+} ions occupy the corners of the unit cell (A-site),

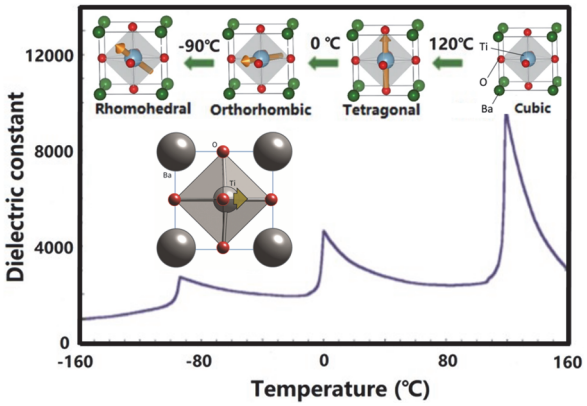

Fig. 7. The relationship between temperature, crystal structure, and the dielectric constant of $BaTiO_3$.

Ti^{4+} ions are located at the body center (B-site), and O^{2-} ions reside at the face centers, forming a highly symmetric framework. The Ti^{4+} ion is octahedrally coordinated by six oxygen ions (forming a TiO_6 octahedron), while the Ba^{2+} ion is 12-fold coordinated. $BaTiO_3$ is a prototypical ABO_3-type ferroelectric ceramic material and serves as a key dielectric in the fabrication of MLCCs. Above its Curie temperature, approximately 120~135°C, $BaTiO_3$ maintains its centrosymmetric cubic phase, exhibiting no spontaneous polarization and relatively low dielectric permittivity. However, as the temperature drops below the Curie point, a phase transition to a tetragonal structure occurs. In this phase, the Ti^{4+} ion displaces slightly from the center of the oxygen octahedron, thereby breaking the inversion symmetry and inducing ferroelectricity. This structural distortion significantly increases the dielectric constant, making the tetragonal phase essential for achieving high capacitance in MLCCs. Upon further cooling, $BaTiO_3$ undergoes successive phase transitions: from tetragonal to orthorhombic near 0°C, and from orthorhombic to rhombohedral at approximately –90°C. Each phase is associated with a unique lattice distortion and domain configuration, leading to changes in the direction of spontaneous polarization and variations in lattice constants. These transitions have a strong influence on the temperature dependence of dielectric properties [31-33]. In MLCCs designed for AI servers and high-performance data centers, it is critically important to enhance volumetric efficiency by employing fine-grained $BaTiO_3$ powders that exhibit a high tetragonality (c/a ratio). For dielectric layers with a thickness of approximately 0.5 μm, the grain size of the sintered $BaTiO_3$

ceramic must be smaller than 100 nm to meet stringent performance and reliability requirements. To fabricate ultrathin MLCCs, dielectric powders must possess nanoscale particle sizes (typically 50–150 nm), high tetragonal phase stability, excellent dispersibility, and narrow particle size distributions. These characteristics are essential to realize high dielectric constants, low dielectric loss, and excellent DC bias stability, which are critical for AI and data-centric power systems operating under high electric fields and temperatures. Studies have demonstrated that precise control of $BaTiO_3$ particle size within the 50~150 nm range is highly effective in stabilizing the tetragonal ferroelectric phase, which in turn enables both high permittivity and a low capacitance variation ratio ($\Delta C/C$) across operating conditions. Within this size regime, the spontaneous polarization is well maintained, and the dielectric response remains sharp and stable, even under miniaturized configurations. In advanced MLCCs designed for AI servers and high-performance data centers, various synthesis methods are employed to produce nanoscale $BaTiO_3$ powders, including solid-state reaction, hydrothermal synthesis, sol-gel processing, and oxalate coprecipitation. Among these, the solid-state reaction method is widely adopted in industry due to its simplicity, scalability, cost-effectiveness, and equipment reliability. However, this method generally requires high processing temperatures exceeding 1,000°C and often results in coarse particles with non-uniform phase composition. Despite these drawbacks, its ease of operation makes it suitable for mass production, though further advancements are necessary to achieve finer particles with enhanced tetragonality. Hydrothermal and sol-gel methods offer significant advantages in producing fine $BaTiO_3$ powders with excellent particle size control at relatively low processing temperatures. Nevertheless, both methods are prone to introducing structural defects, such as residual hydroxyl groups, which can degrade the dielectric performance of the material. The oxalate coprecipitation method provides high phase purity and uniform particle distribution, but its high processing cost and complexity limit its feasibility for large-scale industrial applications [34-40]. Ultimately, the development of synthesis techniques capable of producing nanoscale $BaTiO_3$ powders with high tetragonality, excellent dispersibility, and superior phase purity is a critical challenge. These powders are essential for fabricating MLCCs with ultrathin dielectric layers (<0.5 μm), where a minimum of five uniformly distributed grains per layer is required to ensure mechanical and electrical reliability. Furthermore, a comprehensive understanding of how particle size, crystallinity, and defect chemistry influence dielectric behavior is indispensable for the development of next-generation MLCCs that meet the stringent demands of AI computing systems and high-density power architectures.

5. DC BIAS CHARACTERISTICS AND STABILITY ENHANCEMENT STRATEGIES FOR MLCCs

In high-reliability applications such as automotive electronics, AI servers, and satellites, it is critical that MLCCs maintain a minimum level of capacitance for thousands of hours under sustained DC bias. However, predicting capacitance behavior under actual operating conditions remains extremely challenging due to the complex interplay of multiple factors, including material composition, micro-structure, temperature, and electric field strength. $BaTiO_3$-based high-permittivity ceramics exhibit exceptionally high initial dielectric constants, primarily due to spontaneous polarization and domain formation. The nonlinear dielectric response of these ferroelectric materials is largely governed by domain wall motion, polarization rotation, and their intrinsic ability to undergo substantial polarization changes even under relatively small electric fields. These characteristics are typically well illustrated by the polarization–electric field (P–E) hysteresis loop, as shown in Fig. 8. However, as the applied electric field increases, domain wall mobility becomes progressively suppressed, and polarization rotation is constrained, leading to a significant reduction in dielectric permittivity. Consequently, MLCCs exhibit a nonlinear decrease in capacitance under DC bias, as clearly demonstrated in the typical DC bias behavior shown in Fig. 9 [41-44]. Capacitance degradation under DC bias is not governed solely by domain dynamics; it is also strongly influenced by defect formation and charge migration mechanisms. According to the Surface Effect Model, spontaneous polarization (P_s) exists within each grain, with domain orientations varying based on local domain configurations. The orange paths in the model represent electromigration of oxygen vacancies under an applied DC electric field. These vacancies tend to accumulate at domain

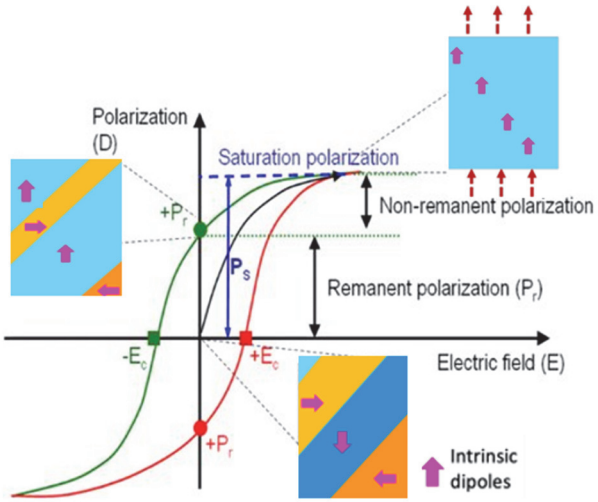

Fig. 8. A representative polarization-electric field (P-E) hysteresis loop for ferroelectric $BaTiO_3$ at room temperature.

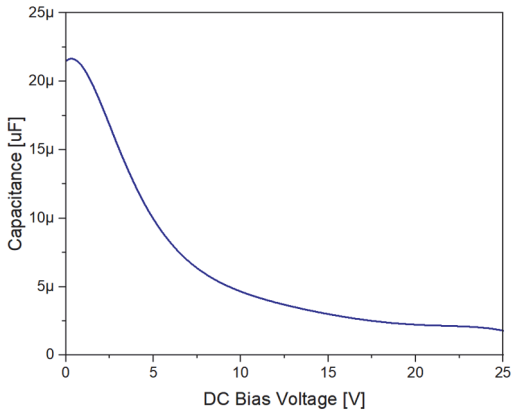

Fig. 9. The characteristic voltage-capacitance (C-V) curve for a $BaTiO_3$-based MLCC.

wall intersections or along grain boundaries, generating localized internal electric fields. These internal fields act to pin domain orientations, thereby hindering domain wall motion and diminishing the dielectric response under bias. In contrast, the Volume Effect Model focuses on defect dipoles formed by the association of acceptor dopants (e.g., Mn) with oxygen vacancies. These dipoles align with local spontaneous polarization and serve to stabilize the domain configuration. However, under prolonged DC bias, the gradual relaxation or migration of these dipoles contributes to long-term degradation of dielectric properties and raises reliability concerns in MLCCs. Conventional strategies to improve DC bias characteristics include doping and grain refinement. For instance, doping $BaTiO_3$ with rare-earth elements such as Y, Dy, or Ho, or refining the grain size to the sub-100 nm scale, disrupts long-range ferroelectric domain alignment, leading to the formation of nano-domains. These structural modifications significantly restrict domain wall mobility, reducing the dielectric response to external electric fields and enhancing DC bias stability. Additionally, finer grains increase the density of grain boundaries, which are regions of lower permittivity and higher dielectric linearity. This so-called "dilution effect" further mitigates nonlinear dielectric responses under bias. However, such approaches come with inherent limitations. Suppressing the activity of ferroelectric domains and increasing the relative fraction of low-permittivity grain boundary regions often leads to a significant reduction in the zero-bias dielectric constant. This drop in initial permittivity translates to lower effective capacitance, presenting a major challenge for next-generation electronic devices that demand both high capacitance and high voltage endurance. Therefore, new material design strategies are required to simultaneously achieve high permittivity and robust DC bias stability. A promising solution to this trade-off is the precision design of core–shell structures. Originally developed to enhance temperature stability, the core–shell architecture has recently gained attention for its effectiveness in improving DC bias performance. Figure 10 provides a comparative analysis of the dielectric properties under varying temperatures and electric fields for two types of $BaTiO_3$-based ceramics. The graph on the left illustrates the typical behavior of a conventional $BaTiO_3$ dielectric, which exhibits a significant degradation in relative permittivity as the applied DC electric field increases from 1 V/mm to 1,000 V/mm. This pronounced drop highlights the poor DC bias characteristic, a critical limitation in high-power applications. In contrast, the graph on the right demonstrates the superior performance of an advanced core-shell structure. In this architecture, each grain consists of a high-permittivity ferroelectric core surrounded by a low-permittivity, linear dielectric shell. The shell layer acts as an electrical buffer, absorbing a substantial portion of the applied voltage and thereby reducing the effective field stress on the core. This mechanism prevents the suppression of domain wall mobility in the core, allowing the material to maintain a stable and high permittivity even under strong electric fields, which is essential for ensuring the

reliability of MLCCs in AI server environments [45-50].

6. DEGRADATION MECHANISMS OF INSULATION RESISTANCE AND RELIABILITY EVALUATION TECHNIQUES IN MLCCs

To achieve higher capacitance, MLCCs have adopted increasingly thinner dielectric layers. While effective in increasing capacitance, this design intensifies the electric field across each layer, which can lower the dielectric breakdown voltage and compromise insulation reliability. Insulation resistance (IR) degradation is governed by both grain boundary conduction (Poole–Frenkel emission at weakened potential barriers) and oxygen vacancy migration (Reduction and Demixing models). AI-grade MLCCs face additional stress due to ultra-thin dielectric layers (<0.3 μm), where localized field intensification accelerates defect-driven conduction. Reliability testing has expanded from HALT (highly accelerated life testing) to include Thermally Stimulated Depolarization Current (TSDC) analysis for quantifying trap states, and the tipping point framework, which predicts breakdown based on oxygen vacancy accumulation thresholds. Weibull lifetime analysis remains standard for statistical reliability assessment, but physics-based models increasingly provide predictive accuracy. Recent approaches involve applying machine learning to leakage current monitoring, enabling real-time failure prediction in data center environments where ppm-level failure rates are demanded. One of the most critical reliability challenges is IR degradation, which is mainly driven by two mechanisms. The first is avalanche breakdown, caused by localized electric field intensification due to non-uniform dielectric layer thickness or microstructural defects in internal electrodes formed during sintering. This concentration of electric field induces localized Joule heating, which can result in thermal runaway and catastrophic dielectric breakdown. The second mechanism is specific to MLCCs with base metal electrode structures, where IR degradation progresses gradually due to the migration of oxygen vacancies under an applied electric field. These vacancies accumulate near the cathode, forming conductive paths that degrade insulation resistance over time [51-54]. To suppress these failure mechanisms, both the microstructure and chemical

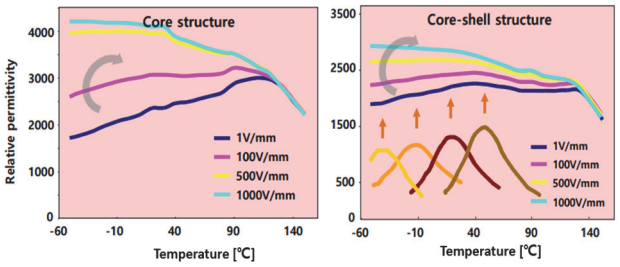

Fig. 10. A comparison of the temperature and electric field-dependent dielectric behavior of $BaTiO_3$ ceramics with a conventional "core structure" versus an advanced "core-shell structure."

composition of the dielectric layer must be carefully controlled. Increasing the number of grains within the dielectric layer helps distribute the electric field more evenly, while reducing grain size alleviates localized field concentrations. However, as dielectric layers approach sub-100 nm thickness, simple grain refinement becomes insufficient, and more sophisticated control over particle size distribution and processing uniformity is required. From a compositional standpoint, mitigating intrinsic degradation pathways is equally important. Several theoretical models have been developed to explain IR degradation mechanisms, including the Grain Boundary Model, the Reduction Model, and the Demixing Model. The Grain Boundary Model attributes slow IR degradation to electric field concentration at grain boundaries, where potential barriers become weakened under high electric fields. Electrons trapped at these barriers can be released through the Poole–Frenkel mechanism, forming conductive paths that progressively reduce insulation resistance. The effectiveness of these barriers is heavily influenced by the concentration of acceptor or amphoteric dopants: higher dopant concentrations reinforce the barriers and inhibit electron migration, while lower concentrations or fewer grain boundaries accelerate degradation. The Reduction Model explains insulation degradation in BME MLCCs by oxygen vacancy generation and migration. During sintering in a reducing atmosphere, oxygen loss forms positively charged vacancies that migrate toward the cathode under an electric field. At the anode, oxygen ions oxidize, producing vacancies and electrons; accumulated vacancies at the cathode form conductive paths causing rapid IR deterioration. Doping $BaTiO_3$ with multivalent acceptors like Mn can delay this by capturing electrons and immobilizing vacancies, but donor

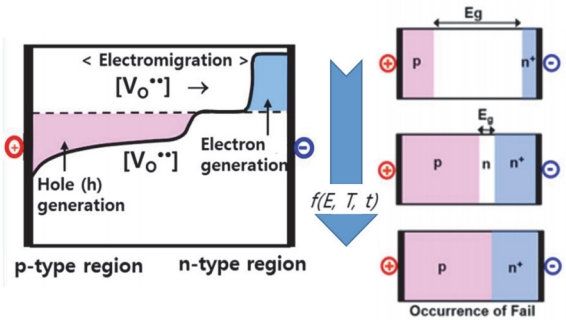

Fig. 11. Schematic illustration of the demixing model.

doping is also needed to control electron concentration and maintain charge neutrality. Figure 11 illustrates the Demixing Model, which describes degradation caused by oxygen vacancy polarization, leading to the formation and expansion of conductive regions. In BME MLCCs, limited oxygen exchange allows the applied electric field to drive the migration of oxygen vacancies and accumulating them near the cathode. As these regions grow toward each other and eventually form a p-n junction, the dielectric abruptly shifts from an insulating to a conductive state, resulting in IR failure. This model accounts for various degradation behaviors depending on dopant type, grain size, and material composition [55-58]. To suppress insulation degradation and ensure long-term reliability of BME MLCCs, a multifaceted strategy is required, involving rare earth doping for dielectric composition control, oxygen vacancy management, grain size optimization, and interface/redox reaction suppression. First, composition design utilizing the site occupancy and amphoteric behavior of rare-earth dopants plays a crucial role in controlling oxygen vacancies. Donor-type ions such as Y^{3+} and Dy^{3+} substitute into the A-site (Ba^{2+}), suppressing vacancy formation, while acceptor-type ions like Yb^{3+} occupy the B-site (Ti^{4+}) and bind with oxygen vacancies, thereby reducing their mobility. Notably, mid-sized ions such as Dy^{3+}, Ho^{3+}, and Er^{3+} can occupy both A- and B-sites, enabling precise donor–acceptor ratio tuning, which simultaneously enhances lattice stability, charge compensation, and insulation performance. Second, oxygen vacancy management is a key technological element in securing insulation reliability. Donor doping suppresses vacancy generation, while acceptor doping facilitates vacancy–dopant complex formation, thereby limiting vacancy migration. Additionally, the cooling rate and atmospheric conditions following re-oxidation critically impact the stabilization of oxygen-related defects and long-term IR stability. Furthermore, grain size engineering is essential to maintaining dielectric performance in ultra-thin MLCC structures. As the thickness of dielectric layers reaches the sub-micrometer level, securing a sufficient number of grains per layer becomes vital to prevent localized breakdown or short-circuiting. To achieve this, advanced techniques for controlling nanoparticle dispersion must be employed. Lastly, interface and redox reaction control are critical considerations. During co-firing and operation, reduction reactions at the interface between the Ni electrode and $BaTiO_3$ dielectricfacilitate oxygen vacancy formation, which can lead to IR degradation and the development of conductive paths. To mitigate this, dopants such as Zr or Dy, which exhibit high resistance to reduction, can be added. Alternatively, nanolayer coatings of SiO_2 or Al_2O_3 on $BaTiO_3$ particles can be used to suppress interfacial reactions with Ni. Furthermore, it is essential to match the sintering shrinkage behavior of $BaTiO_3$ and Ni to prevent the formation of interfacial porosity during co-sintering, thereby improving insulation reliability. Several methods are used to evaluate the reliability of MLCCs, including Thermally Stimulated Depolarization Current (TSDC) analysis, Highly Accelerated Life Testing (HALT), and, more recently, the tipping point framework. TSDC analysis is a highly sensitive technique for characterizing ionic defects, trap states, and space charge dynamics within ceramic dielectrics. In this method, the sample is first pre-polarized under a constant electric field, then the temperature is linearly increased while measuring the resulting depolarization current. This allows for the quantitative analysis of various relaxation processes. Peaks in the current temperature curve correspond to specific trap energy levels or activation energies for defect migration. By analyzing the peak temperature and its dependence on the applied electric field, physical parameters such as oxygen vacancy mobility and concentration can be extracted. This method is particularly useful for $BaTiO_3$ based MLCCs, as it enables the evaluation of the thermodynamic behavior of oxygen vacancies and related charge compensation mechanisms. Highly Accelerated Life Testing (HALT) is a traditional and widely used method that subjects MLCCs to extreme stress conditions—such as high temperature and voltage—to accelerate degradation and failure mechanisms. The resulting failure time data are typically fitted to Weibull distributions to determine shape

Table 2. Reliability and environmental conditions for MLCCs used in consumer, industrial, automotive, and AI server/data center applications.

Item	Consumer	Industrial	Automotive	AI Server / Data Center
Operating Temperature	0°C to 40°C	-10°C to 70°C	-40°C to 85/155°C	-10°C to 105°C (max 125°C)
Service Life	1–3 years	5–10 years	Up to 15 years	24/7 operation, over 10 years
Humidity Resistance	Low	Standard environment	0–100% RH	Must pass 85°C/85% RH THB test
Field Failure Rate	<10%	<<1%	Target: 0 ppm	Target: 0 ppm
Technical Documentation	None	Conditional	Mandatory	Mandatory (capacitance/IR drift, THB, etc.)
Supply Stability	None	Up to 5 years	Up to 30 years	Over 10 years, multi-vendor sourcing system

parameters and characteristic lifetimes. The Arrhenius model is also employed to estimate lifetime based on activation energy, temperature, and electric field. However, the model's reliance on an empirically derived field acceleration factor and its limited physical grounding reduce its accuracy when extrapolating long-term reliability. Despite these limitations, HALT remains a critical tool for initial design validation as well as quality and reliability assurance. More recently, the tipping point framework has emerged as a promising alternative to traditional empirical lifetime models. This approach defines a critical threshold for dielectric degradation based on the cumulative accumulation of mobile oxygen vacancies. Once this threshold is reached, dielectric breakdown occurs, driven by space charge formation and the development of leakage current paths. Unlike empirical models, this framework is grounded in a clear physical mechanism, offering greater predictive accuracy. It has demonstrated strong reproducibility in forecasting failure times across a wide range of electric field strengths and temperatures. As such, the tipping point framework is gaining recognition as a powerful tool for lifetime prediction in high-reliability MLCC applications—including AI servers and automotive systems—and is expected to become a foundational component of future MLCC design and reliability assurance methodologies [59-61].

7. PERFORMANCE REQUIREMENTS AND MARKET TRENDS IN AI MLCCs

Compared to automotive-grade MLCCs, AI-grade MLCCs prioritize electrical performance attributes such as high-speed response, electric field stability, and mounting efficiency to meet the stringent demands of next-generation computing platforms. Table 2 summarizes the reliability and environmental requirements for MLCCs used in consumer, industrial, automotive, and AI server/data center applications. As of 2024, the market size for AI and data center MLCCs is estimated at approximately USD 17.2 million, with projections reaching USD 45 million by 2032, corresponding to a compound annual growth rate (CAGR) of 12.8%. This growth is driven by the rapid expansion of AI servers and data centers, increasing deployment of high-performance GPUs, TPUs, and ASICs, and a rising demand for passive components optimized for high-power, high-frequency, and fast-transient environments. Key application areas include high-performance AI accelerators such as the NVIDIA H100 and Google TPU v5, as well as AI-integrated devices like Microsoft Copilot-enabled PCs. These platforms require significantly more MLCCs—typically around 18,000 to 20,000 units per system—which is approximately 5 to 12.5 times higher than in conventional servers. A representative use case is in power supply units (PSUs), where high-voltage MLCCs are deployed in LLC resonant circuits and snubber networks. These capacitors must withstand voltages ranging from several hundred to several thousand volts while maintaining DC bias stability and minimizing capacitance drift due to temperature variations. High-capacitance MLCCs located near GPUs, CPUs, and TPUs are used for load compensation, where they must handle rapid current spikes and prevent voltage droop through ultra-fast charge/discharge response, low equivalent series inductance (ESL), and reliable

performance in high-temperature environments often exceeding 105°C. Typical specifications include rated voltages between 2.5 V and 4 V, with capacitance values of at least 47 μF for 0402-size packages and 100 μF or more for 0603-size packages. Emerging technological trends in AI-grade MLCCs include sub-500 nm dielectric and internal electrode layering, advanced reliability testing protocols, high-density mounting near processors, enhanced thermal dissipation structures, and optimization of both electrical/mechanical robustness and power delivery efficiency. Due to the extreme computational density of AI servers and data centers—which typically operate continuously (24/7/365)—the reliability and supply chain requirements for AI-grade MLCCs exceed those of consumer, industrial, and even automotive applications. Among the critical reliability requirements, thermal tolerance is paramount. Local temperatures near voltage regulator modules (VRMs) and GPUs often exceed 100°C—well above the 70°C limit of consumer-grade MLCCs. To ensure reliable performance under such thermal stress, AI-grade MLCCs must utilize thermally stable dielectric materials such as X8R or X9R, which support continuous operation at temperatures up to 125°C. Long-term electrical and thermal stability is essential, as AI servers are expected to maintain full functionality over lifespans exceeding 10 years, aligning with or surpassing automotive-grade reliability standards. Frequent voltage and current transients during AI training and inference cycles further necessitate capacitors with stable capacitance, IR), and ripple current endurance under sustained stress. Humidity resistance is also a critical parameter. Despite the controlled HVAC environments in data centers, localized condensation can occur near high-speed fans. As a result, AI-grade MLCCs must pass Temperature-Humidity Bias (THB) tests of at least 1,000 hours at 85°C and 85% relative humidity to ensure long-term moisture durability. An ultra-low field failure rate is mandatory. While consumer-grade MLCCs may tolerate field failure rates below 10% and industrial-grade below 1%, AI-grade components must achieve failure rates below 1 ppm (0.0001%), as even a single capacitor failure can lead to a complete system shutdown. Accordingly, component suppliers must provide detailed Return Trend Reports (RTRs) and in-depth failure analysis documentation. Finally, comprehensive technical documentation is required for AI-grade MLCCs. This includes data on capacitance and IR drift over time, results from THB and High Temperature Reverse Bias (HTRB) testing, soldering temperature profiles, Material Safety Data Sheets (MSDS), RoHS and REACH compliance certifications, and structured digital data formats such as XML or JSON to support system-level simulation and predictive reliability modeling.

8. CONCLUSION

The advancement of AI servers and high-performance computing systems has led to a sharp increase in demand for passive components suitable for high-power consumption and high-density circuit environments. In such environments, MLCCs capable of maintaining long-term stable performance under high temperature, high voltage, and high current conditions are indispensable. This paper has outlined the key technical requirements and recommended specifications for MLCCs used in AI systems, and proposed future directions for technological development. MLCCs used in AI servers are required to operate for over 10 years under high-temperature conditions: approximately 105°C in fanless and IoT systems, around 95°C in AI computing environments, and approximately 75°C in network equipment such as switches and routers. To ensure stable electrical performance under these conditions, the equivalent series resistance (ESR) must be maintained below 10 mΩ, the equivalent series inductance (ESL) below 0.5 nH, and the transient response time within 100 ps. Moreover, since X7R dielectrics can suffer up to an 80% reduction in capacitance due to DC bias effects, improved dielectric stability technologies are necessary. From a structural perspective, there must be no cracks or visual defects in high-density multilayer structures, and structural integrity must be validated through SAT (scanning acoustic tomography) standards. The most urgent technical challenge is suppressing capacitance loss under DC bias conditions, which requires optimization of dielectric composition and microstructure. In parallel, the implementation of ultra-compact MLCCs for high-density systems demands precision sintering technologies that can reduce dielectric layer thickness to below 0.5 μm, along with ESR/ESL minimization technologies for 0402 and smaller case sizes. Furthermore, to mitigate derating effects, optimized voltage design strategies involving thicker dielectric layers are needed, and ultra-low

ESL structures must be designed to withstand high-speed transient loads (on the order of 100 A/μs) as found in GPU and TPU applications. In conclusion, MLCCs for AI servers must go beyond merely providing capacitance—they must ensure reliability and stability under extreme conditions of temperature, voltage, frequency, and current. To achieve this, advancements are required in highly reliable dielectric materials, miniaturized designs, enhanced DC bias stability, and ultra-low ESR/ESL structures. Future R&D efforts should focus on achieving integrated MLCC technologies that can simultaneously satisfy these multi-faceted requirements through innovations in dielectric material design, manufacturing process optimization, and degradation-resistant structural engineering.

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